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| EXAMINER |
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ELLIS, RICHARD L

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2183

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

MAILED

Application Number: 09/954,596
Filing Date: September 12, 2001
Appellant(s): GUNZINGER, ANTON

MAY 03 2005

Technology Center 2100

Carl Oppedahl
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 22, 2005.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Claimed Subject Matter*

The summary of claimed subject matter contained in the brief is correct.

(6) *Grounds of rejection to be reviewed on appeal*

The appellant's statement of the grounds of rejection to be reviewed on appeal in the brief is correct.

(7) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

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(8) Prior Art of Record

5,117,350

Parrish et al.

May 26, 1992

Specification of co-pending application 07/232,155, incorporated by reference into Parrish et al.'s specification at col. 4 lines 3-8

Definitions from "Yahoo! Education", The Dictionary of Computers, Information Processing & Telecommunications, second edition, Modern Dictionary of Electronics, and Microsoft Press Computer Dictionary, second edition, cited as extrinsic evidence to applicant in paper number 20040913, mailed September 21, 2004.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Construction

As an initial matter, applicant in his arguments in the brief relies on a special, secret, definition of the term "message-passing communications network" in his attempt to argue supposed differences between the **claimed** invention and the applied reference to Parrish et al. However, this special secret definition for "message-passing communications network" is not present in either the claim language or in the specification nor is it set forth with any clarity in the arguments.

The claim language itself provides no definition for the term "message-passing communications network", but merely uses the term in the assumption that a reader understands the meaning of the term.

Furthermore, it has been well established that it is the claim language which defines the invention:

Claimed subject matter, **not** the specification, is the measure of invention. Limitations in the specification **cannot** be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978).

"It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field,

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but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be **confused with adding an extraneous limitation** appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is **not** to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

In the present case, because the claim language itself provides no specific meaning for the term "message-passing communications network" one must then look to the specification to determine if the specification provides any enlightenment as to what applicant may have meant by that term. However, in this application, when one looks to the specification, one finds that "message-passing communications network" is never recited anywhere within the specification. The various constituent words of "message-passing communications network" are recited in isolation, but the claim term "message-passing communications network" is never utilized. The specification, which consists of a total of 10 pages, utilizes the terms "message-passing", "communications network", "network", and "message" as summarized in the following table:

| <i>Term</i> | <i>Number of occurrences</i> | <i>Location of occurrences</i> |
|-----------------------|------------------------------|--|
| message-passing | 1 | page 2 line 15 |
| communication network | 4 | page 4 line 5 page 4 line 7 page 5 line 21 page 6 lines 7-8 |
| network | 3 | page 4 lines 9 and 12 page 10 line 1 |
| message | 1 | page 4 line 19 |

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The constituent terms are recited in the following contexts:

"message-passing":

"Message-passing systems are more scalable; systems having up to 10,000 processors have been built. However, as a rule they present difficulties when being programmed and low latencies can be achieved only by means of special operating systems." (page 2 lines 14-17)

This paragraph provides no definition of "message-passing" beyond an ethereal indication that such systems are "more scalable". The passage then continues on to indicate that such systems have difficulties that are only curable by use of special operating systems.

"communications network":

"A parallel computer system contains n processing elements, $1', 1'' \dots 1^n$, where $n = 2, 3 \dots$ and is a natural number equal to or larger than 2. These at least two processor elements are connected to one another by a shared communications network 0 appropriately evincing wide bandwidth and low latency. No assumptions are made concerning the communications network. Illustratively "Fast Ethernet", ATM, GigaBit Ethernet, Fiber Channel or any other fast network may be used." (page 4 lines 2-9)

"Figure 2 shows the configuration of a computer system of the invention. In this instance too this is a parallel computer system comprising n processor elements $1', 1'' \dots 1^n$, where $n = 1, 2 \dots$ and is a natural number. These processor elements are connected to each other by a common communications network 0 appropriately evincing a large bandwidth and low latency." (page 5 lines 17-22)

"In the method of the invention, the processor writes the results of its computations into the communications manager unit ($6'$ or $6'' \dots 6^n$ (200'). Said unit adds a global address. The data values and the address are transferred to the communications unit $4'$ (201') and, passing through the conventional communications network 0 (201'), arrive at the communications units $4', 4'' \dots 4^n$ (202" ... 202")." (page 6 lines 3-9)

"network":

"No assumptions are made concerning the communications network. Illustratively "Fast Ethernet", ATM, GigaBit Ethernet, Fiber Channel or any other fast network may be used. Again no assumptions are made concerning topology; buses, stars rings, 2-D or 3-D networks (torus) may be used, or any other topology. The costs and performances of such networks differ and must be matched to needs.

"If the network supports point-point, multicast and broadcast, the whole concept can make use of this functionality to reduce communication." (page 10 lines 1-3)

The above passages provide no explicit definition of the term "network" beyond a clear indication by applicant that a conventional well known prior art network is suitable for use in the invention: ("Illustratively "Fast Ethernet", ATM, GigaBit Ethernet, Fiber Channel or any other fast network may be used.", "passing through the conventional communications network"). I.e., a network such as the one disclosed in the copending application incorporated by reference into Parrish et. al.

"message":

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"A message exchange takes place as follows": (page 4 lines 19-20)

This scant usage of the term "message" above can hardly be found to provide any definition for the term "message".

Therefore, because as shown above the specification does not provide any additional definition for the constituent terms of the claimed term "message-passing communications network" it also does not provide any explicit definition for that term in the claims.

"The specification merely describes in a general fashion certain features and capabilities desirable in a portable computer. This description, however, is far from establishing a specialized definition restricting the claimed invention to a computer having a specific set of characteristics and capabilities." *In re Paulsen*, 31 USPQ2d 1671, 1674-75 (Fed. Cir. 1994)

Accordingly, the only possible meaning that can be properly applied to that claim term is the term's ordinary meaning to one of skill in the art:

[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997)

Extrinsic evidence was previously cited to applicant in paper number 20040913, mailed September 21, 2004 supporting the examiner's understanding of the ordinary meaning of the term "message-passing communications network" as such "would be understood by one of ordinary skill in the art". The following definitions are found from that extrinsic evidence:

| <i>Term</i> | <i>Definition</i> | <i>Source</i> |
|------------------|---|--|
| network | <u>Computer Science</u> A system of computers interconnected by telephone wires or other means in order to share information. | Yahoo! Education |
| computer network | a complex consisting of two or more interconnected computing units. | Dictionary of Computers, Information Processing, and Telecommunications, 2nd edition |
| network | (1) an interconnected group of nodes. | Dictionary of Computers, Information Processing, and Telecommunications, 2nd edition |

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| <i>Term</i> | <i>Definition</i> | <i>Source</i> |
|-------------|--|---|
| network | 3. An organization of stations with a capability for intercommunication, although not necessarily on the same channel. | Modern Dictionary of Electronics |
| network | A group of computers and associated devices that are connected by communications facilities. ... Some types of communication are simple user-to-user messages; | Microsoft Press Computer Dictionary, second edition |

Accordingly, as seen from the definitions above, a "network" is a group of computing systems interconnected for communications. Therefore, the claimed term "communications network" is actually redundant, because "network" already means "for communications". "Message-passing" is defined as passing (exchanging) messages between users (see Microsoft Press definition for network). Accordingly, a "message-passing communications network" is any group of computers interconnected for communications via the exchange of messages.

Additionally, applicant is also operating under the belief that the claimed term "not solely" means exclusively. However, as shown from the extrinsic evidence from Yahoo! Education the term solely is defined to mean:

"Solely: 1. Alone; singly: *solely responsible*. 2. Entirely; exclusively: *did it solely for love*."

As seen from the definition, the term "solely" already means "exclusively". Therefore, when prefixed with the word "not" as applicant has done in the claims, the result is that the meaning for the claimed term "not solely" is "not exclusively", "not alone", "not singly", i.e., not limited to only one thing or to only one method of operation. I.e., a system such as the network disclosed in the copending application incorporated by reference into Parrish et. al. where the network provides for both bus type data exchange transactions and message passing network transactions.

Claim rejection

Claims 16-31 and 33-34 are rejected under 37 USC 102(b) as being clearly anticipated by Parrish et al. U.S. Patent 5,117,350. The specification of co-pending application 07/232,155 was incorporated by reference into Parrish et al.'s specification at col. 4 lines 3-8. Definitions from "Yahoo! Education", *The Dictionary of Computers, Information Processing & Telecommunications*, second edition, *Modern Dictionary of Electronics*, and *Microsoft Press Computer Dictionary*, second edition were cited as extrinsic evidence to applicant in paper number 20040913, mailed September 21, 2004.

| | |
|----------|--|
| Claim 16 | |
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| Claim 16 | |
|---|--|
| 16. A method of operating a parallel computer system | fig. 2, showing two nodes (NODE A, NODE B) of a parallel computer system (col. 8 lines 3-13) |
| having at least first and second processor elements, | fig. 2, 100, 120, col. 8 lines 3-5 and 13-14 |
| each processor element comprising a processor, | col. 14 lines 10-11 |
| a local program memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 |
| a local data memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 (the program and data share the memory in Parrish et al.'s system) |
| a communications manager | fig. 5a-5b, 219, 239, col. 13 lines 21-25, fig. 8b-8d, 419, 439, 459, col. 14 lines 13-24 |
| and an operating system, | col. 15 lines 30-31 |
| within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; | fig. 2, 115, 116, 135, 136, showing the elements interconnected by "VME Bus" and "VSB Bus" fig. 8b-8d, 401, 421, 441, showing a "computer bus" which interconnects with the remainder of the system as shown on fig. 2 but omitted from fig. 8 to avoid confusion. Both the "VME Bus" (115, 135) and the "VSB Bus" (116, 136) are connected in common to the local program memories, local data memories, and communications managers of the respective nodes (100, 120) as seen from fig. 2. Additionally, col. 8 lines 13-19 states that Parrish et al. considers the "VME Bus" and "VSB Bus" to together comprise the local "computer bus" which is shown on figs. 4-8. |

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| Claim 16 | |
|---|---|
| the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network; | <p>fig. 2 160, 4a-4c 160, 5a-5b, 260, 5a-5b, 360, fig. 8b-8d, 460, the interconnect bus being disclosed in co-pending application 07/232,155 (incorporated by reference at col. 4 lines 3-8 of Parrish et al.) and defined as a message-passing communications network at page 12 lines 4-8 of the co-pending application: ("The present invention concerns a synchronous, time multiplexed, parallel bus architecture which operates in an open-loop broadcast mode and is capable of supporting <u>both</u> transaction process and <u>message process</u> communications among plural functional units.")</p> <p>As shown from the claim construction section above, Parrish et al.'s bus is a "communications network" (a group of computers and associated devices that are connected by communications facilities [INTERCONNECT BUS]) that operates by "message-passing" (Parrish et al. explicitly defines the bus as operating in a "message process" in the co-pending application).</p> <p>Additionally, as best applicant's special secret definition for "message-passing communications network" can be determined from the lack of definition in the specification, it appears that applicant's definition is that of an interconnect that transfers data via messages. In this case, Parrish et al.'s system continues to anticipate the claims because Parrish et al.'s interconnect bus is an interconnect (it interconnects several independent computers) that allows data transfer to happen via messages (Parrish et al. explicitly defines the bus as operating in a message passing manner in the co-pending application).</p> |
| the processor elements each executing an application; | col. 13 lines 35-36 |
| each communications manager further containing a plurality of predefined values | fig. 8b-8d, element 419, containing six, 439, containing four, and 459 containing ten predefined values respectively. |
| each of which, in the event of a match of one of the predetermined values to a global address in a message, | col. 13 lines 49-68, note specifically "to check to see if address 356K were located in an active partition". In order "to check to see" the system is "matching" addresses. |
| causes storage of results of an associated computation in local data memory; | col. 13 lines 49-68, note specifically lines 62-67, where a "local bus memory write would be issued". |

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| Claim 16 | |
|--|---|
| the method comprising the steps of: writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element; | col. 13 lines 49-54, note specifically "be detected by address translation hardware". This "address translation hardware is present within the communications manager as seen from fig. 5a-5b, 219, 239 and as such this "detection" is a "writing into the communications manager". |
| adding, by the communications manager, a global address to the result of the computation; | col. 13 lines 54-58, "system address 356K (605) is the "global address" because it is the address of the data in the global "system memory space" (620) of fig. 7. Element 630 of fig. 7 translated local address 2148K into global address 356K, therefore, element 630 "added" the global address. |
| propagating, on the message-passing communications network, a message comprising the global address and the result of the computation; | 460, col. 13 lines 58-60, the "system memory space" of fig. 7 corresponds to element 480 of fig. 8 and as seen from fig. 8 is interconnected to the node (400) via the "INTERCONNECT BUS" which as detailed above, is a "message-passing communications network". The data value which was written to local address 2148K at col. 13 lines 54-56 is the "result of a computation". Transmission of the message via the bus results in "propagation" of the message. |
| receiving the message, via the message-passing communications network, by the communications manager of the second processor element; | 460, col. 13 lines 58-60, see also fig. 7 where element 640 receives the value and translates the global address back into a local address for Node B. |
| comparing, by the communications manager of the second processor element, the global address in the message with the predefined value for a match; | col. 13 lines 58-62, Node B's system bus interface is receiving the message from the network, and "checking" to see if the address is in a partition allocated to Node B. This is "comparing" the global address with the values in element 459. |
| in the event of a match, computing a local address by the communications manager of the second processor element, | col. 13 lines 62-68, global address 356K is translated into local address 868K. This is "computing a local address" by the communications manager (640, 459) |
| and storing the results of the computation at the local address via the common bus to the local data memory. | col. 13 lines 62-68, a local bus memory write is issued. This is "storing the results ... at the local address". |

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| Claim 17 | |
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| Claim 17 | |
|---|---|
| 17. The method of claim 16 wherein the predefined values are further characterized as comprising an address window, | fig. 8, DCM1, DCM2, SGM1, RGM1, note that DCM1 is defined to extend from 512K to 768K, SGM1 extends from 2048K to 2816K, etc. These are "address windows" because they are ranges of addresses. |
| each window comprising an initial address and an end address. | DCM1 of Node A begins at address 512K and ends at address 768K, other address windows have their own corresponding beginning and ending addresses. |
| A match comprising the global address falling between the initial address and the end address. | col. 13 lines 49-52, showing that the system checks for addresses falling between the start and end points of the windows. |

| Claim 18 | |
|--|---|
| 18. The method of claim 16 wherein computing a local address comprises adding an offset of one or more bits to the global address, yielding the local address. | col. 13 lines 60-68, in order to translate into a local address, Parrish et al.'s system must have added a correcting offset to the global address to generate the local address. |

| Claim 19 | |
|--|--|
| 19. The method of claim 16 wherein computing a local address comprises replacing one or more bits of the global address by a base value, yielding the local address. | col. 13 lines 60-68, in order to "translate" the global address to the local address, Parrish et al.'s system must eventually replace bits of the supplied global address with other bits derived from the starting address of the window in order to arrive at the local address value. |

| Claim 20 | |
|---|---|
| 20. The method of claim 16 wherein the propagating step comprises propagating the message to a number of processor elements, the number comprising less than all and more than one of the processor elements. | fig. 8b-8d, DCM2 is allocated in two (Node A and Node C) out of three of the exemplary nodes. Accordingly, an access to DCM2 will be propagated to two nodes (Node A and Node c), but not to all three nodes (col. 12 lines 10-35). Two is less than all (three) and more than one. |

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| Claim 21 | |
|---|--|
| 21. A parallel computer system | fig. 2, showing two nodes (NODE A, NODE B) of a parallel computer system (col. 8 lines 3-13) |
| having at least first and second processor elements, | fig. 2, 100, 120, col. 8 lines 3-5 and 13-14 |
| each processor element comprising a processor, | col. 14 lines 10-11 |
| a local program memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 |
| a local data memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 (the program and data share the memory in Parrish et al.'s system) |
| a communications manager | fig. 5a-5b, 219, 239, col. 13 lines 21-25, fig. 8b-8d, 419, 439, 459, col. 14 lines 13-24 |
| and an operating system, | col. 15 lines 30-31 |
| within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; | fig. 2, 115, 116, 135, 136, showing the elements interconnected by "VME Bus" and "VSB Bus" fig. 8b-8d, 401, 421, 441, showing a "computer bus" which interconnects with the remainder of the system as shown on fig. 2 but omitted from fig. 8 to avoid confusion. Both the "VME Bus" (115, 135) and the "VSB Bus" (116, 136) are connected in common to the local program memories, local data memories, and communications managers of the respective nodes (100, 120) as seen from fig. 2. Additionally, col. 8 lines 13-19 states that Parrish et al. considers the "VME Bus" and "VSB Bus" to together comprise the local "computer bus" which is shown on figs. 4-8. |
| the local data memories of the at least first and second processor elements not on a common bus; | figs. 8b-8d, the local memories of each node (Node A, Node B, Node C) are not connected to a common bus, but instead to separate buses (401, 421, 441) internal to each node (see fig. 2). |

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| Claim 21 | |
|--|---|
| <p>the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network;</p> | <p>fig. 2 160, 4a-4c 160, 5a-5b, 260, 5a-5b, 360, fig. 8b-8d, 460, the interconnect bus being disclosed in co-pending application 07/232,155 (incorporated by reference at col. 4 lines 3-8 of Parrish et al.) and defined as a message-passing communications network at page 12 lines 4-8 of the co-pending application: ("The present invention concerns a synchronous, time multiplexed, parallel bus architecture which operates in an open-loop broadcast mode and is capable of supporting both transaction process and message process communications among plural functional units.")</p> <p>As shown from the claim construction section above, Parrish et al.'s bus is a "communications network" (a group of computers and associated devices that are connected by communications facilities [INTERCONNECT BUS]) that operates by "message-passing" (Parrish et al. explicitly defines the bus as operating in a "message process" in the co-pending application).</p> <p>Additionally, as best applicant's special secret definition for "message-passing communications network" can be determined from the lack of definition in the specification, it appears that applicant's definition is that of an interconnect that transfers data via messages. In this case, Parrish et al.'s system continues to anticipate the claims because Parrish et al.'s interconnect bus is an interconnect (it interconnects several independent computers) that allows data transfer to happen via messages (Parrish et al. explicitly defines the bus as operating in a message passing manner in the co-pending application).</p> |
| <p>the processor elements each executing an application;</p> | <p>col. 13 lines 35-36</p> |
| <p>each communications manager further containing a plurality of predefined values</p> | <p>fig. 8b-8d, element 419, containing six, 439, containing four, and 459 containing ten predefined values respectively.</p> |
| <p>each of which, in the event of a match of one of the predetermined values to a global address in a message,</p> | <p>col. 13 lines 49-68, note specifically "to check to see if address 356K were located in an active partition". In order "to check to see" the system is "matching" addresses.</p> |
| <p>causes storage of results of an associated computation in local data memory;</p> | <p>col. 13 lines 49-68, note specifically lines 62-67, where a "local bus memory write would be issued".</p> |

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| Claim 21 | |
|---|---|
| for each communications manager the communications manager comprising first means responsive to writing, by the processor of the processor element by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element, | col. 13 lines 49-54, note specifically "be detected by address translation hardware". This "address translation hardware is present within the communications manager as seen from fig. 5a-5b, 219, 239 and as such this "detection" is a "writing into the communications manager". |
| by adding a global address to the result of the computation, | col. 13 lines 54-58, "system address 356K (605) is the "global address" because it is the address of the data in the global "system memory space" (620) of fig. 7. Element 630 of fig. 7 translated local address 2148K into global address 356K, therefore, element 630 "added" the global address. |
| and by propagating, on the message-passing communications network, a message comprising the global address and the result of the computation; | 460, col. 13 lines 58-60, the "system memory space" of fig. 7 corresponds to element 480 of fig. 8 and as seen from fig. 8 is interconnected to the node (400) via the "INTERCONNECT BUS" which as detailed above, is a "message-passing communications network". The data value which was written to local address 2148K at col. 13 lines 54-56 is the "result of a computation". Transmission of the message via the bus results in "propagation" of the message. |
| for each communications manager, the communications manager comprising second means responsive to receiving a message, via the message-passing communications network, by the communications manager, | 460, col. 13 lines 58-60, see also fig. 7 where element 640 receives the value and translates the global address back into a local address for Node B. |
| for comparing the global address in the message with the plurality of predefined values for a match, | col. 13 lines 58-62, Node B's system bus interface is receiving the message from the network, and "checking" to see if the address is in a partition allocated to Node B. This is "comparing" the global address with the values in element 459. |
| in the event of a match, for computing a local address, | col. 13 lines 62-68, global address 356K is translated into local address 868K. This is "computing a local address" by the communications manager (640, 459) |
| and storing the results of the computation at the local address via the common bus to the local data memory. | col. 13 lines 62-68, a local bus memory write is issued. This is "storing the results ... at the local address". |

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| Claim 22 | |
|--|---|
| 22. The apparatus of claim 21 wherein the predefined values are further characterized as comprising an address window, | fig. 8, DCM1, DCM2, SGM1, RGM1, note that DCM1 is defined to extend from 512K to 768K, SGM1 extends from 2048K to 2816K, etc. These are "address windows" because they are ranges of addresses. |
| each window comprising an initial address and an end address, | DCM1 of Node A begins at address 512K and ends at address 768K, other address windows have their own corresponding beginning and ending addresses. |
| a match comprising the global address falling between the initial address and the end address. | col. 13 lines 49-52, showing that the system checks for addresses falling between the start and end points of the windows. |

| Claim 23 | |
|--|---|
| 23. The apparatus of claim 21 wherein the second means computes a local address by adding an offset of one or more bits to the global address, yielding the local address. | col. 13 lines 60-68, in order to translate into a local address, Parrish et al.'s system must have added a correcting offset to the global address to generate the local address. |

| Claim 24 | |
|--|--|
| 24. The apparatus of claim 21 wherein the second means computes a local address by replacing one or more bits of the global address by a base value, yielding the local address. | col. 13 lines 60-68, in order to "translate" the global address to the local address, Parrish et al.'s system must eventually replace bits of the supplied global address with other bits derived from the starting address of the window in order to arrive at the local address value. |

| Claim 25 | |
|--|---|
| 25. The apparatus of claim 21 wherein the first means propagates the message to a number of processor elements, the number comprising less than all and more than one of the processor elements. | fig. 8b-8d, DCM2 is allocated in two (Node A and Node C) out of three of the exemplary nodes. Accordingly, an access to DCM2 will be propagated to two nodes (Node A and Node c), but not to all three nodes (col. 12 lines 10-35). Two is less than all (three) and more than one. |

| Claim 26 | |
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| Claim 26 | |
|---|--|
| 26. A method of operating a parallel computer system | fig. 2, showing two nodes (NODE A, NODE B) of a parallel computer system (col. 8 lines 3-13) |
| having at least first and second processor elements. | fig. 2, 100, 120, col. 8 lines 3-5 and 13-14 |
| each processor element comprising a processor, | col. 14 lines 10-11 |
| a local program memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 |
| a local data memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 (the program and data share the memory in Parrish et al.'s system) |
| a communications manager | fig. 5a-5b, 219, 239, col. 13 lines 21-25, fig. 8b-8d, 419, 439, 459, col. 14 lines 13-24 |
| and an operating system, | col. 15 lines 30-31 |
| within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; | fig. 2, 115, 116, 135, 136, showing the elements interconnected by "VME Bus" and "VSB Bus" fig. 8b-8d, 401, 421, 441, showing a "computer bus" which interconnects with the remainder of the system as shown on fig. 2 but omitted from fig. 8 to avoid confusion. Both the "VME Bus" (115, 135) and the "VSB Bus" (116, 136) are connected in common to the local program memories, local data memories, and communications managers of the respective nodes (100, 120) as seen from fig. 2. Additionally, col. 8 lines 13-19 states that Parrish et al. considers the "VME Bus" and "VSB Bus" to together comprise the local "computer bus" which is shown on figs. 4-8. |

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| Claim 26 | |
|--|---|
| <p>the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network;</p> | <p>fig. 2 160, 4a-4c 160, 5a-5b, 260, 5a-5b, 360, fig. 8b-8d, 460, the interconnect bus being disclosed in co-pending application 07/232,155 (incorporated by reference at col. 4 lines 3-8 of Parrish et al.) and defined as a message-passing communications network at page 12 lines 4-8 of the co-pending application: ("The present invention concerns a synchronous, time multiplexed, parallel bus architecture which operates in an open-loop broadcast mode and is capable of supporting both transaction process and message process communications among plural functional units.")</p> <p>As shown from the claim construction section above, Parrish et al.'s bus is a "communications network" (a group of computers and associated devices that are connected by communications facilities [INTERCONNECT BUS]) that operates by "message-passing" (Parrish et al. explicitly defines the bus as operating in a "message process" in the co-pending application).</p> <p>Additionally, as best applicant's special secret definition for "message-passing communications network" can be determined from the lack of definition in the specification, it appears that applicant's definition is that of an interconnect that transfers data via messages. In this case, Parrish et al.'s system continues to anticipate the claims because Parrish et al.'s interconnect bus is an interconnect (it interconnects several independent computers) that allows data transfer to happen via messages (Parrish et al. explicitly defines the bus as operating in a message passing manner in the co-pending application).</p> |
| <p>the processor elements each executing an application;</p> | <p>col. 13 lines 35-36</p> |
| <p>each communications manager further containing a plurality of predefined values</p> | <p>fig. 8b-8d, element 419, containing six, 439, containing four, and 459 containing ten predefined values respectively.</p> |
| <p>each of which, in the event of a match of one of the predetermined values to a global address in a message,</p> | <p>col. 13 lines 49-68, note specifically "to check to see if address 356K were located in an active partition". In order "to check to see" the system is "matching" addresses.</p> |
| <p>causes storage of results of an associated computation in local data memory;</p> | <p>col. 13 lines 49-68, note specifically lines 62-67, where a "local bus memory write would be issued".</p> |

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| Claim 26 | |
|--|---|
| the method comprising the steps of: writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element; | col. 13 lines 49-54, note specifically "be detected by address translation hardware". This "address translation hardware is present within the communications manager as seen from fig. 5a-5b, 219, 239 and as such this "detection" is a "writing into the communications manager". |
| adding, by the communications manager, a global address to the result of the computation; | col. 13 lines 54-58, "system address 356K (605) is the "global address" because it is the address of the data in the global "system memory space" (620) of fig. 7. Element 630 of fig. 7 translated local address 2148K into global address 356K, therefore, element 630 "added" the global address. |
| propagating, on the message-passing communications network, a message comprising the global address and the result of the computation; | 460, col. 13 lines 58-60, the "system memory space" of fig. 7 corresponds to element 480 of fig. 8 and as seen from fig. 8 is interconnected to the node (400) via the "INTERCONNECT BUS" which as detailed above, is a "message-passing communications network". The data value which was written to local address 2148K at col. 13 lines 54-56 is the "result of a computation". Transmission of the message via the bus results in "propagation" of the message. |
| receiving the message, via the message-passing communications network, by the communications manager of the second processor element; | 460, col. 13 lines 58-60, see also fig. 7 where element 640 receives the value and translates the global address back into a local address for Node B. |
| comparing, by the communications manager of the second processor element, the global address in the message with the predefined values for a match; | col. 13 lines 58-62, Node B's system bus interface is receiving the message from the network, and "checking" to see if the address is in a partition allocated to Node B. This is "comparing" the global address with the values in element 459. |
| in the event of a match, computing a local address by the communications manager of the second processor element, | col. 13 lines 62-68, global address 356K is translated into local address 868K. This is "computing a local address" by the communications manager (640, 459) |
| and storing the results of the computation at the local address via the common bus to the local data memory, | col. 13 lines 62-68, a local bus memory write is issued. This is "storing the results ... at the local address". |

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| Claim 26 | |
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| wherein the predefined values are further characterized as comprising an address window, | fig. 8, DCM1, DCM2, SGM1, RGM1, note that DCM1 is defined to extend from 512K to 768K, SGM1 extends from 2048K to 2816K, etc. These are "address windows" because they are ranges of addresses. |
| each window comprising an initial address and an end address, | DCM1 of Node A begins at address 512K and ends at address 768K, other address windows have their own corresponding beginning and ending addresses. |
| a match comprising the global address falling between the initial address and the end address. | col. 13 lines 49-52, showing that the system checks for addresses falling between the start and end points of the windows. |

| Claim 27 | |
|---|--|
| 27. A method of operating a parallel computer system | fig. 2, showing two nodes (NODE A, NODE B) of a parallel computer system (col. 8 lines 3-13) |
| having at least first and second processor elements, | fig. 2, 100, 120, col. 8 lines 3-5 and 13-14 |
| each processor element comprising a processor, | col. 14 lines 10-11 |
| a local program memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 |
| a local data memory. | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 (the program and data share the memory in Parrish et al.'s system) |
| a communications manager | fig. 5a-5b, 219, 239, col. 13 lines 21-25, fig. 8b-8d, 419, 439, 459, col. 14 lines 13-24 |
| and an operating system, | col. 15 lines 30-31 |
| within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; | fig. 2, 115, 116, 135, 136, showing the elements interconnected by "VME Bus" and "VSB Bus" fig. 8b-8d, 401, 421, 441, showing a "computer bus" which interconnects with the remainder of the system as shown on fig. 2 but omitted from fig. 8 to avoid confusion. Both the "VME Bus" (115, 135) and the "VSB Bus" (116, 136) are connected in common to the local program memories, local data memories, and communications managers of the respective nodes (100, 120) as seen from fig. 2. Additionally, col. 8 lines 13-19 states that Parrish et al. considers the "VME Bus" and "VSB Bus" to together comprise the local "computer bus" which is shown on figs. 4-8. |

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| Claim 27 | |
|--|---|
| <p>the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network;</p> | <p>fig. 2 160, 4a-4c 160, 5a-5b, 260, 5a-5b, 360, fig. 8b-8d, 460, the interconnect bus being disclosed in co-pending application 07/232,155 (incorporated by reference at col. 4 lines 3-8 of Parrish et al.) and defined as a message-passing communications network at page 12 lines 4-8 of the co-pending application: ("The present invention concerns a synchronous, time multiplexed, parallel bus architecture which operates in an open-loop broadcast mode and is capable of supporting both transaction process and message process communications among plural functional units.")</p> <p>As shown from the claim construction section above, Parrish et al.'s bus is a "communications network" (a group of computers and associated devices that are connected by communications facilities [INTERCONNECT BUS]) that operates by "message-passing" (Parrish et al. explicitly defines the bus as operating in a "message process" in the co-pending application).</p> <p>Additionally, as best applicant's special secret definition for "message-passing communications network" can be determined from the lack of definition in the specification, it appears that applicant's definition is that of an interconnect that transfers data via messages. In this case, Parrish et al.'s system continues to anticipate the claims because Parrish et al.'s interconnect bus is an interconnect (it interconnects several independent computers) that allows data transfer to happen via messages (Parrish et al. explicitly defines the bus as operating in a message passing manner in the co-pending application).</p> |
| <p>the processor elements each executing an application;</p> | <p>Col. 13 lines 35-36</p> |
| <p>each communications manager further containing a plurality of predefined values</p> | <p>fig. 8b-8d, element 419, containing six, 439, containing four, and 459 containing ten predefined values respectively.</p> |
| <p>each of which, in the event of a match of one of the predetermined values to a global address in a message,</p> | <p>col. 13 lines 49-68, note specifically "to check to see if address 356K were located in an active partition". In order "to check to see" the system is "matching" addresses.</p> |
| <p>causes storage of results of an associated computation in local data memory;</p> | <p>col. 13 lines 49-68, note specifically lines 62-67, where a "local bus memory write would be issued".</p> |

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| Claim 27 | |
|---|---|
| the method comprising the steps of: writing, by the processor of the first processor element by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element; | col. 13 lines 49-54, note specifically "be detected by address translation hardware". This "address translation hardware is present within the communications manager as seen from fig. 5a-5b, 219, 239 and as such this "detection" is a "writing into the communications manager". |
| adding, by the communications manager, a global address to the result of the computation; | col. 13 lines 54-58, "system address 356K (605) is the "global address" because it is the address of the data in the global "system memory space" (620) of fig. 7. Element 630 of fig. 7 translated local address 2148K into global address 356K, therefore, element 630 "added" the global address. |
| propagating, on the message-passing communications network, a message comprising the global address and the result of the computation; | 460, col. 13 lines 58-60, the "system memory space" of fig. 7 corresponds to element 480 of fig. 8 and as seen from fig. 8 is interconnected to the node (400) via the "INTERCONNECT BUS" which as detailed above, is a "message-passing communications network". The data value which was written to local address 2148K at col. 13 lines 54-56 is the "result of a computation". Transmission of the message via the bus results in "propagation" of the message. |
| receiving the message, via the message-passing communications network, by the communications manager of the second processor element; | 460, col. 13 lines 58-60, see also fig. 7 where element 640 receives the value and translates the global address back into a local address for Node B. |
| comparing, by the communications manager of the second processor element, the global address in the message with the predefined values for a match; | col. 13 lines 58-62, Node B's system bus interface is receiving the message from the network, and "checking" to see if the address is in a partition allocated to Node B. This is "comparing" the global address with the values in element 459. |
| in the event of a match, computing a local address by the communications manager of the second processor element, | col. 13 lines 62-68, global address 356K is translated into local address 868K. This is "computing a local address" by the communications manager (640, 459) |
| and storing the results of the computation at the local address via the common bus to the local data memory, | col. 13 lines 62-68, a local bus memory write is issued. This is "storing the results ... at the local address". |

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| Claim 27 | |
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| wherein the propagating step comprises propagating the message to a number of processor elements, the number comprising less than all and more than one of the processor elements. | fig. 8b-8d, DCM2 is allocated in two (Node A and Node C) out of three of the exemplary nodes. Accordingly, an access to DCM2 will be propagated to two nodes (Node A and Node c), but not to all three nodes (col. 12 lines 10-35). Two is less than all (three) and more than one. |

| Claim 28 | |
|---|--|
| 28. A parallel computer system | fig. 2, showing two nodes (NODE A, NODE B) of a parallel computer system (col. 8 lines 3-13) |
| having at least first and second processor elements, | fig. 2, 100, 120, col. 8 lines 3-5 and 13-14 |
| each processor element comprising a processor, | col. 14 lines 10-11 |
| a local program memory. | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 |
| a local data memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 (the program and data share the memory in Parrish et al.'s system) |
| a communications manager | fig. 5a-5b, 219, 239, col. 13 lines 21-25, fig. 8b-8d, 419, 439, 459, col. 14 lines 13-24 |
| and an operating system, | col. 15 lines 30-31 |
| within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; | fig. 2, 115, 116, 135, 136, showing the elements interconnected by "VME Bus" and "VSB Bus" fig. 8b-8d, 401, 421, 441, showing a "computer bus" which interconnects with the remainder of the system as shown on fig. 2 but omitted from fig. 8 to avoid confusion. Both the "VME Bus" (115, 135) and the "VSB Bus" (116, 136) are connected in common to the local program memories, local data memories, and communications managers of the respective nodes (100, 120) as seen from fig. 2. Additionally, col. 8 lines 13-19 states that Parrish et al. considers the "VME Bus" and "VSB Bus" to together comprise the local "computer bus" which is shown on figs. 4-8. |
| the local data memories of the at least first and second processor elements not on a common bus; | figs. 8b-8d, the local memories of each node (Node A, Node B, Node C) are not connected to a common bus, but instead to separate buses (401, 421, 441) internal to each node (see fig. 2). |

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| Claim 28 | |
|--|---|
| <p>the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network;</p> | <p>fig. 2 160, 4a-4c 160, 5a-5b, 260, 5a-5b, 360, fig. 8b-8d, 460, the interconnect bus being disclosed in co-pending application 07/232,155 (incorporated by reference at col. 4 lines 3-8 of Parrish et al.) and defined as a message-passing communications network at page 12 lines 4-8 of the co-pending application: ("The present invention concerns a synchronous, time multiplexed, parallel bus architecture which operates in an open-loop broadcast mode and is capable of supporting both transaction process and message process communications among plural functional units.")</p> <p>As shown from the claim construction section above, Parrish et al.'s bus is a "communications network" (a group of computers and associated devices that are connected by communications facilities [INTERCONNECT BUS]) that operates by "message-passing" (Parrish et al. explicitly defines the bus as operating in a "message process" in the co-pending application).</p> <p>Additionally, as best applicant's special secret definition for "message-passing communications network" can be determined from the lack of definition in the specification, it appears that applicant's definition is that of an interconnect that transfers data via messages. In this case, Parrish et al.'s system continues to anticipate the claims because Parrish et al.'s interconnect bus is an interconnect (it interconnects several independent computers) that allows data transfer to happen via messages (Parrish et al. explicitly defines the bus as operating in a message passing manner in the co-pending application).</p> |
| <p>the processor elements each executing an application;</p> | <p>col. 13 lines 35-36</p> |
| <p>each communications manager further containing a plurality of predefined values</p> | <p>fig. 8b-8d, element 419, containing six, 439, containing four, and 459 containing ten predefined values respectively.</p> |
| <p>each of which, in the event of a match of one of the predetermined values to a global address in a message,</p> | <p>col. 13 lines 49-68, note specifically "to check to see if address 356K were located in an active partition". In order "to check to see" the system is "matching" addresses.</p> |
| <p>causes storage of results of an associated computation in local data memory;</p> | <p>col. 13 lines 49-68, note specifically lines 62-67, where a "local bus memory write would be issued".</p> |

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| Claim 28 | |
|---|---|
| for each communications manager, the communications manager comprising first means responsive to writing, by the processor of the processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element, | col. 13 lines 49-54, note specifically "be detected by address translation hardware". This "address translation hardware is present within the communications manager as seen from fig. 5a-5b, 219, 239 and as such this "detection" is a "writing into the communications manager". |
| by adding a global address to the result of the computation, | col. 13 lines 54-58, "system address 356K (605) is the "global address" because it is the address of the data in the global "system memory space" (620) of fig. 7. Element 630 of fig. 7 translated local address 2148K into global address 356K, therefore, element 630 "added" the global address. |
| and by propagating, on the message-passing communications network, a message comprising the global address and the result of the computation; | 460, col. 13 lines 58-60, the "system memory space" of fig. 7 corresponds to element 480 of fig. 8 and as seen from fig. 8 is interconnected to the node (400) via the "INTERCONNECT BUS" which as detailed above, is a "message-passing communications network". The data value which was written to local address 2148K at col. 13 lines 54-56 is the "result of a computation". Transmission of the message via the bus results in "propagation" of the message. |
| for each communications manager, the communications manager comprising second means responsive to receiving a message, via the message-passing communications network, by the communications manager, | 460, col. 13 lines 58-60, see also fig. 7 where element 640 receives the value and translates the global address back into a local address for Node B. |
| for comparing the global address in the message with the predefined values for a match, | col. 13 lines 58-62, Node B's system bus interface is receiving the message from the network, and "checking" to see if the address is in a partition allocated to Node B. This is "comparing" the global address with the values in element 459. |
| in the event of a match, for computing a local address, | col. 13 lines 62-68, global address 356K is translated into local address 868K. This is "computing a local address" by the communications manager (640, 459) |

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| Claim 28 | |
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| and storing the results of the computation at the local address via the common bus to the local data memory, | col. 13 lines 62-68, a local bus memory write is issued. This is "storing the results ... at the local address". |
| wherein the predefined values are further characterized as comprising an address window, | fig. 8, DCM1, DCM2, SGM1, RGM1, note that DCM1 is defined to extend from 512K to 768K, SGM1 extends from 2048K to 2816K, etc. These are "address windows" because they are ranges of addresses. |
| each window comprising an initial address and an end address, | DCM1 of Node A begins at address 512K and ends at address 768K, other address windows have their own corresponding beginning and ending addresses. |
| a match comprising the global address falling between the initial address and the end address. | col. 13 lines 49-52, showing that the system checks for addresses falling between the start and end points of the windows. |

| Claim 29 | |
|--|--|
| 29. A parallel computer system | fig. 2, showing two nodes (NODE A, NODE B) of a parallel computer system (col. 8 lines 3-13) |
| having at least first and second processor elements, | fig. 2, 100, 120, col. 8 lines 3-5 and 13-14 |
| each processor element comprising a processor, | col. 14 lines 10-11 |
| a local program memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 |
| a local data memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 (the program and data share the memory in Parrish et al.'s system) |
| a communications manager | fig. 5a-5b, 219, 239, col. 13 lines 21-25, fig. 8b-8d, 419, 439, 459, col. 14 lines 13-24 |
| and an operating system, | col. 15 lines 30-31 |

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| Claim 29 | |
|---|---|
| within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; | fig. 2, 115, 116, 135, 136, showing the elements interconnected by "VME Bus" and "VSB Bus" fig. 8b-8d, 401, 421, 441, showing a "computer bus" which interconnects with the remainder of the system as shown on fig. 2 but omitted from fig. 8 to avoid confusion. Both the "VME Bus" (115, 135) and the "VSB Bus" (116, 136) are connected in common to the local program memories, local data memories, and communications managers of the respective nodes (100, 120) as seen from fig. 2. Additionally, col. 8 lines 13-19 states that Parrish et al. considers the "VME Bus" and "VSB Bus" to together comprise the local "computer bus" which is shown on figs. 4-8. |
| the local data memories of the at least first and second processor elements not on a common bus; | figs. 8b-8d, the local memories of each node (Node A, Node B, Node C) are not connected to a common bus, but instead to separate buses (401, 421, 441) internal to each node (see fig. 2). |
| the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network; | <p>fig. 2 160, 4a-4c 160, 5a-5b, 260, 5a-5b, 360, fig. 8b-8d, 460, the interconnect bus being disclosed in co-pending application 07/232,155 (incorporated by reference at col. 4 lines 3-8 of Parrish et al.) and defined as a message-passing communications network at page 12 lines 4-8 of the co-pending application: ("The present invention concerns a synchronous, time multiplexed, parallel bus architecture which operates in an open-loop broadcast mode and is capable of supporting both transaction process and message process communications among plural functional units.")</p> <p>As shown from the claim construction section above, Parrish et al.'s bus is a "communications network" (a group of computers and associated devices that are connected by communications facilities [INTERCONNECT BUS]) that operates by "message-passing" (Parrish et al. explicitly defines the bus as operating in a "message process" in the co-pending application).</p> <p>Additionally, as best applicant's special secret definition for "message-passing communications network" can be determined from the lack of definition in the specification, it appears that applicant's definition is that of an interconnect that transfers data via messages. In this case, Parrish et al.'s system continues to anticipate the claims because Parrish et al.'s interconnect bus is an interconnect (it interconnects several independent computers) that allows data transfer to happen via messages (Parrish et al. explicitly defines the bus as operating in a message passing manner in the co-pending application).</p> |
| the processor elements each executing an application; | col. 13 lines 35-36 |

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| Claim 29 | |
|--|---|
| each communications manager further containing a plurality of predefined values each of | fig. 8b-8d, element 419, containing six, 439, containing four, and 459 containing ten predefined values respectively. |
| which, in the event of a match of one of the predetermined values to a global address in a message, | col. 13 lines 49-68, note specifically "to check to see if address 356K were located in an active partition". In order "to check to see" the system is "matching" addresses. |
| causes storage of results of an associated computation in local data memory; | col. 13 lines 49-68, note specifically lines 62-67, where a "local bus memory write would be issued". |
| for each communications manager, the communications manager comprising first means responsive to writing, by the processor of the processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element | col. 13 lines 49-54, note specifically "be detected by address translation hardware". This "address translation hardware is present within the communications manager as seen from fig. 5a-5b, 219, 239 and as such this "detection" is a "writing into the communications manager". |
| by adding a global address to the result of the computation, | col. 13 lines 54-58, "system address 356K (605) is the "global address" because it is the address of the data in the global "system memory space" (620) of fig. 7. Element 630 if fig. 7 translated local address 2148K into global address 356K, therefore, element 630 "added" the global address. |
| and by propagating, on the message-passing communications network, a message comprising the global address and the result of the computation; | 460, col. 13 lines 58-60, the "system memory space" of fig. 7 corresponds to element 480 of fig. 8 and as seen from fig. 8 is interconnected to the node (400) via the "INTERCONNECT BUS" which as detailed above, is a "message-passing communications network". The data value which was written to local address 2148K at col. 13 lines 54-56 is the "result of a computation". Transmission of the message via the bus results in "propagation" of the message. |
| for each communications manager, the communications manager comprising second means responsive to receiving a message, via the message-passing communications network, by the communications manager, | 460, col. 13 lines 58-60, see also fig. 7 where element 640 receives the value and translates the global address back into a local address for Node B. |

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| Claim 29 | |
|--|---|
| for comparing the global address in the message with the predefined values for a match, | col. 13 lines 58-62, Node B's system bus interface is receiving the message from the network, and "checking" to see if the address is in a partition allocated to Node B. This is "comparing" the global address with the values in element 459. |
| in the event of a match, for computing a local address, | col. 13 lines 62-68, global address 356K is translated into local address 868K. This is "computing a local address" by the communications manager (640, 459) |
| and storing the results of the computation at the local address via the common bus to the local data memory, | col. 13 lines 62-68, a local bus memory write is issued. This is "storing the results ... at the local address". |
| wherein the first means propagates the message to a number of processor elements, the number comprising less than all and more than one of the processor elements. | fig. 8b-8d, DCM2 is allocated in two (Node A and Node C) out of three of the exemplary nodes. Accordingly, an access to DCM2 will be propagated to two nodes (Node A and Node c), but not to all three nodes (col. 12 lines 10-35). Two is less than all (three) and more than one. |

| Claim 30 | |
|--|--|
| 30. The method of claim 16 wherein the predefined values are further characterized as comprising at least two address windows, | fig. 8b-8d, address windows DCM1, DCM2, SGM1, are all present in Node A |
| each window comprising an initial address and an end address, | DCM1 begins at 512K and ends at 768K, DCM2 begins at 768K and ends at 1280K, SGM1 begins at 2048K and ends at 2304K |
| a match comprising the global address falling between the initial address and the end address of at least one of the at least two address windows. | col. 13 lines 49-68, showing that the system checks for addresses that fall between the defined start and end points of the appropriate windows. |

| Claim 31 | |
|---|---|
| 31. The apparatus of claim 21 wherein the predefined values are further characterized as comprising at least two address windows, | fig. 8b-8d, address windows DCM1, DCM2, SGM1, are all present in Node A |

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| Claim 31 | |
|--|--|
| each window comprising an initial address and an end address, | DCM1 of Node A begins at address 512K and ends at address 768K, other address windows have their own corresponding beginning and ending addresses. |
| a match comprising the global address falling between the initial address and the end address of at least one of the at least two address windows. | col. 13 lines 49-68, showing that the system checks for addresses that fall between the defined start and end points of the appropriate windows. |

| Claim 33 | |
|---|--|
| 33. A method of operating a parallel computer system | fig. 2, showing two nodes (NODE A, NODE B) of a parallel computer system (col. 8 lines 3-13) |
| having at least first and second processor elements, | fig. 2, 100, 120, col. 8 lines 3-5 and 13-14 |
| each processor element comprising a processor, | col. 14 lines 10-11 |
| a local program memory | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 |
| a local data memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 (the program and data share the memory in Parrish et al.'s system) |
| a communications manager | fig. 5a-5b, 219, 239, col. 13 lines 21-25, fig. 8b-8d, 419, 439, 459, col. 14 lines 13-24 |
| and an operating system, | col. 15 lines 30-31 |
| within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; | fig. 2, 115, 116, 135, 136, showing the elements interconnected by "VME Bus" and "VSB Bus" fig. 8b-8d, 401, 421, 441, showing a "computer bus" which interconnects with the remainder of the system as shown on fig. 2 but omitted from fig. 8 to avoid confusion. Both the "VME Bus" (115, 135) and the "VSB Bus" (116, 136) are connected in common to the local program memories, local data memories, and communications managers of the respective nodes (100, 120) as seen from fig. 2. Additionally, col. 8 lines 13-19 states that Parrish et al. considers the "VME Bus" and "VSB Bus" to together comprise the local "computer bus" which is shown on figs. 4-8. |

| Claim 33 | |
|---|---|
| <p>the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network and not solely by a common bus;</p> | <p>As seen from the cited definition of the term "solely" the word means "alone; singly; entirely; or exclusively". Therefore, the claim language construct "not solely by a common bus" means "not exclusively, not alone, not singly, by a common bus". As was detailed above, Parrish et al. indicated that his particular bus was unique in that it was both a message passing network as well as a common bus. Therefore, because Parrish et al.'s disclosed bus was both a message passing network as well as a bus, it was "not exclusively a common bus", i.e., not limited to only functioning as a common bus, and therefore was "not solely a common bus" as claimed.</p> <p>However, this is also an alternate interpretation of applicant's claim language construct. Applicant recites a "common bus" within the claims as interconnecting the local program memory, local data memory, and communications managers of each node. This therefore is equivalent to Parrish et al.'s "Computer bus" disclosed in figs. 4-6 and 8 which Parrish et al. has defined at col. 8 lines 13-19 as encompassing both the VME Bus and VSB Bus of fig. 2. Applicant then claims that the communications managers are interconnected by a second interconnect, termed "message passing communications network" in the claims, and not solely by a common bus. Applicant's arguments indicate that applicant's intent for "not solely by a common bus" is for this term to further limit the "message passing communications network". However a literal interpretation of the claim language would have this "not solely" term potentially referencing the already cited "common bus" of the claims. In this interpretation, applicant's claim language would be claiming that the communications managers were interconnected by two buses, one called "common", and another called "message-passing communications network". Given this possible alternate interpretation, Parrish et al. continues to read upon the claim language because the communications managers of Parrish et al. are connected to both a common bus (Computer bus of figs 4-6 and 8) and to a message-passing communications network (Interconnect bus of figs. 4-6 and 8).</p> |
| <p>the processor elements each executing an application;</p> | <p>col. 13 lines 35-36</p> |
| <p>each communications manager further containing a plurality of predefined values</p> | <p>fig. 8b-8d, element 419, containing six, 439, containing four, and 459 containing ten predefined values respectively.</p> |

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| Claim 33 | |
|--|--|
| each of which, in the event of a match of one of the predetermined values to a global address in a message, | col. 13 lines 49-68, note specifically "to check to see if address 356K were located in an active partition". In order "to check to see" the system is "matching" addresses. |
| causes storage of results of an associated computation in local data memory; | col. 13 lines 49-68, note specifically lines 62-67, where a "local bus memory write would be issued". |
| the method comprising the steps of: writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element; | col. 13 lines 49-54, note specifically "be detected by address translation hardware". This "address translation hardware is present within the communications manager as seen from fig. 5a-5b, 219, 239 and as such this "detection" is a "writing into the communications manager". |
| adding, by the communications manager, a global address to the result of the computation; | col. 13 lines 54-58, "system address 356K (605) is the "global address" because it is the address of the data in the global "system memory space" (620) of fig. 7. Element 630 of fig. 7 translated local address 2148K into global address 356K, therefore, element 630 "added" the global address. |
| propagating, on the message-passing communications network and not solely by a common bus, a message comprising the global address and the result of the computation; | As shown above, Parrish et al.'s bus is "not solely a common bus" and propagation was shown at 460, col. 13 lines 58-60, the "system memory space" of fig. 7 corresponds to element 480 of fig. 8 and as seen from fig. 8 is interconnected to the node (400) via the "INTERCONNECT BUS" which as detailed above, is a "message-passing communications network". The data value which was written to local address 2148K at col. 13 lines 54-56 is the "result of a computation". Transmission of the message via the bus results in "propagation" of the message. |
| receiving the message, via the message-passing communications network and not solely by a common bus, by the communications manager of the second processor element; | As shown above, Parrish et al.'s bus is "not solely a common bus" and receiving a message was shown by element 640 of fig. 7 receiving the message and translating to a local address. |
| comparing, by the communications manager of the second processor element, the global address in the message with the predefined values for a match; | col. 13 lines 58-62, Node B's system bus interface is receiving the message from the network, and "checking" to see if the address is in a partition allocated to Node B. This is "comparing" the global address with the values in element 459. |

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| Claim 33 | |
|---|--|
| in the event of a match, computing a local address by the communications manager of the second processor element, | col. 13 lines 62-68, global address 356K is translated into local address 868K. This is "computing a local address" by the communications manager (640, 459) |
| and storing the results of the computation at the local address via the common bus to the local data memory. | col. 13 lines 62-68, a local bus memory write is issued. This is "storing the results ... at the local address". |

| Claim 34 | |
|---|--|
| 34. A parallel computer system | fig. 2, showing two nodes (NODE A, NODE B) of a parallel computer system (col. 8 lines 3-13) |
| having at least first and second processor elements, | fig. 2, 100, 120, col. 8 lines 3-5 and 13-14 |
| each processor element comprising a processor, | col. 14 lines 10-11 |
| a local program memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 |
| a local data memory, | fig. 2, IPM, col. 8 lines 13-19 and col. 14 lines 11-12 and 13-16 (the program and data share the memory in Parrish et al.'s system) |
| a communications manager | fig. 5a-5b, 219, 239, col. 13 lines 21-25, fig. 8b-8d, 419, 439, 459, col. 14 lines 13-24 |
| and an operating system, | col. 15 lines 30-31 |
| within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus; | fig. 2, 115, 116, 135, 136, showing the elements interconnected by "VME Bus" and "VSB Bus" fig. 8b-8d, 401, 421, 441, showing a "computer bus" which interconnects with the remainder of the system as shown on fig. 2 but omitted from fig. 8 to avoid confusion. Both the "VME Bus" (115, 135) and the "VSB Bus" (116, 136) are connected in common to the local program memories, local data memories, and communications managers of the respective nodes (100, 120) as seen from fig. 2. Additionally, col. 8 lines 13-19 states that Parrish et al. considers the "VME Bus" and "VSB Bus" to together comprise the local "computer bus" which is shown on figs. 4-8. |
| the local data memories of the at least first and second processor elements not on a common bus; | figs. 8b-8d, the local memories of each node (Node A, Node B, Node C) are not connected to a common bus, but instead to separate buses (401, 421, 441) internal to each node (see fig. 2). |

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| Claim 34 | |
|--|---|
| <p>the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network;</p> | <p>fig. 2 160, 4a-4c 160, 5a-5b, 260, 5a-5b, 360, fig. 8b-8d, 460, the interconnect bus being disclosed in co-pending application 07/232,155 (incorporated by reference at col. 4 lines 3-8 of Parrish et al.) and defined as a message-passing communications network at page 12 lines 4-8 of the co-pending application: ("The present invention concerns a synchronous, time multiplexed, parallel bus architecture which operates in an open-loop broadcast mode and is capable of supporting both transaction process and message process communications among plural functional units.")</p> <p>As shown from the claim construction section above, Parrish et al.'s bus is a "communications network" (a group of computers and associated devices that are connected by communications facilities [INTERCONNECT BUS]) that operates by "message-passing" (Parrish et al. explicitly defines the bus as operating in a "message process" in the co-pending application).</p> <p>Additionally, as best applicant's special secret definition for "message-passing communications network" can be determined from the lack of definition in the specification, it appears that applicant's definition is that of an interconnect that transfers data via messages. In this case, Parrish et al.'s system continues to anticipate the claims because Parrish et al.'s interconnect bus is an interconnect (it interconnects several independent computers) that allows data transfer to happen via messages (Parrish et al. explicitly defines the bus as operating in a message passing manner in the co-pending application).</p> |
| <p>the processor elements each executing an application;</p> | <p>col. 13 lines 35-36</p> |
| <p>each communications manager further containing a plurality of predefined values</p> | <p>fig. 8b-8d, element 419, containing six, 439, containing four, and 459 containing ten predefined values respectively.</p> |
| <p>each of which, in the event of a match of one of the predetermined values to a global address in a message,</p> | <p>col. 13 lines 49-68, note specifically "to check to see if address 356K were located in an active partition". In order "to check to see" the system is "matching" addresses.</p> |
| <p>causes storage of results of an associated computation in local data memory;</p> | <p>col. 13 lines 49-68, note specifically lines 62-67, where a "local bus memory write would be issued".</p> |

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| Claim 34 | |
|---|--|
| for each communications manager, the communications manager comprising first means responsive to writing, by the processor of the processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element, | col. 13 lines 49-54, note specifically "be detected by address translation hardware". This "address translation hardware is present within the communications manager as seen from fig. 5a-5b, 219, 239 and as such this "detection" is a "writing into the communications manager". |
| by adding a global address to the result of the computation, | col. 13 lines 54-58, "system address 356K (605) is the "global address" because it is the address of the data in the global "system memory space" (620) of fig. 7. Element 630 of fig. 7 translated local address 2148K into global address 356K, therefore, element 630 "added" the global address. |
| and by propagating, on the message-passing communications network and not solely by a common bus, | As shown above, Parrish et al.'s bus is "not solely a common bus" and propagation was shown at 460, col. 13 lines 58-60, the "system memory space" of fig. 7 corresponds to element 480 of fig. 8 and as seen from fig. 8 is interconnected to the node (400) via the "INTERCONNECT BUS" which as detailed above, is a "message-passing communications network". The data value which was written to local address 2148K at col. 13 lines 54-56 is the "result of a computation". Transmission of the message via the bus results in "propagation" of the message. |
| a message comprising the global address and the result of the computation; | col. 13 lines 49-52, this "write" being "the result", col. 13 lines 52-58, the system memory address 356k comprising the "global address", the write occurring by "the result" and "the global address" being forwarded over the interconnect bus (fig. 5 260, fig. 8 460) to the system memory space. Therefore, the "message" on the "interconnect bus" contains both "the result" and "the global address". |
| for each communications manager, the communications manager comprising second means responsive to receiving a message, via the message-passing communications network and not solely by a common bus, by the communications manager, | As shown above, Parrish et al.'s bus is "not solely a common bus" and receiving a message was shown by element 640 of fig. 7 receiving the message and translating to a local address. |

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| Claim 34 | |
|--|--|
| for comparing the global address in the message with the plurality of predefined values for a match, | col. 13 lines 58-62, Node B's system bus interface is receiving the message from the network, and "checking" to see if the address is in a partition allocated to Node B. This is "comparing" the global address with the values in element 459. |
| in the event of a match, for computing a local address, | col. 13 lines 62-68, global address 356K is translated into local address 868K. This is "computing a local address" by the communications manager (640, 459) |
| and storing the results of the computation at the local address via the common bus to the local data memory. | col. 13 lines 62-68, a local bus memory write is issued. This is "storing the results ... at the local address". |

(10) Response to Argument

On page 13 of the arguments, applicant argues:

"The most important distinction is that in the claimed invention, there is an express limitation that the processor elements are coupled by means of a message-passing communications network. In contrast, the processor elements of Parris [sic] are coupled by means of a bus."

This is not found persuasive because as seen from the claim construction section, *supra.*, the term that applicant is arguing has only the plain meaning of its constituent terms, which is a set of computing systems (Node A, Node B, Node C) connected for communications (INTERCONNECT BUS) via exchange of messages (co-pending application 07/232,155 at page 12 lines 4-8). Accordingly, Parrish et al.'s bus is exactly applicant's claimed "message-passing communications network" because it interconnects nodes for communications via the exchange of messages.

On page 13 of the brief, applicant argues:

"By way of background it is mentioned that as is well known to those skilled in the art, a message-passing network is more complex and is different from a simple bus. For example, scalability is greater for a message-passing network, and sub-grounds and sub-networks can be

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established. In a bus, mutual influences can happen such as interference and contention for the medium."

This is not found persuasive because this is part of applicant's special secret definition for "message-passing communication network", which as shown in the claim construction section, *supra.*, is not present anywhere within the claim language, specification, or arguments.

Additionally, applicant has merely made the assertion that this special secret definition is well known, but has provided no concrete evidence with which to back up his assertion. However, it is also noted that were applicant to attempt to supply any concrete evidence in a reply brief, such evidence would be insufficient to alter the definition of "message-passing communications network":

"Absent an express definition in their specification, the fact that appellants can point to definitions or usages that conform to their interpretation does not make the PTO's definition unreasonable when the PTO can point to other sources that support its interpretation." *In re Morris*, 44 USPQ2d 1023, 1029 (Fed. Cir. 1997)

Furthermore, as detailed above in the rejection of the claims, Parrish et al.'s bus is indeed a "message-passing communication network" because it is an interconnect among a group of nodes for communication via the exchange of messages.

On page 14 of the brief, applicant argues:

"The Parrish reference teaches a bus oriented system. The bus structure of the Parrish references allows message passing processes. However, in Parrish, all processor elements (which the Examiner equates to Parrish's "functional units") are on a common bus. Parrish, therefore, does not teach a message-passing communications network. A one-dimensional structure such as a bus is not a network according to a usual definition."

This is not found persuasive because this is an additional instance of applicant's reliance upon a special secret definition for "message-passing communications network". As was shown in the claim construction section, *supra.*, at no point does the accepted definition of "network" as

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known by one of ordinary skill in the art exclude a one-dimensional structure such as a bus from the definition of "network". A network is simply "a system of computers interconnected by telephone wires or other means in order to share information". In no way does the "usual definition" of network exclude one-dimensional structures from "network". Applicant is again relying upon this special secret definition known only to him, and not disclosed anywhere within the specification and claims. Furthermore, as detailed numerous times above in the rejection of the claims, as best applicant's term "message passing communications bus" can be understood, Parrish et al.'s disclosed Interconnect bus operates in an identical manner.

On page 14 of the brief, applicant argues:

"In a bus-oriented system, only one message may be transmitted at one time. In a communications network, hundreds or thousands of messages may be in transit at the same time. The claimed method is therefore much more complex than a bus-oriented system such as that of Parrish."

This is not found persuasive because applicant is again relying upon his special secret definition of network. As is clearly evident from the claim construction section, the usual definition of network makes no requirement for some number of messages greater than one to be in transit at the same time in order to qualify a system as a "communications network". While applicant may very well have invented an outstanding networking system, his specification is totally silent as to the particulars of that networking system, and as such, these secret special definitions of "network" can not be utilized to differentiate the claimed system from the prior art.

"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

Except that in the present application, even applicant's written description is silent as to

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this supposed "outstanding" network that applicant believes his system contains. Therefore, applicant can not rely upon this secret definition to define the claim language away from the applied reference.

On page 17 of the brief, applicant argues:

"The Examiner has expressed the view that this claim 16 is "clearly anticipated" by Parrish. But for the reasons discussed above (a message-passing communications network is not a bus) it is requested that this rejection be reversed."

This is not found persuasive because as discussed above in the responses to pages 13-14 of the brief, applicant's special secret definition of "message-passing communication network" can not be relied upon to differentiate the claimed system from the cited reference. When "message-passing communications network" is given it's broadest reasonable interpretation in light of the lack of definition by the claims, specification, and arguments, it is seen as shown above in the claim construction section and claim rejection section to be anticipated by the "INTERCONNECT BUS" disclosed by Parrish et al.

On page 17 of the brief, applicant argues:

"The undersigned has been unable to find this limitation [propagating the message to a number of processor elements, the number comprising less than all and more than one of the processor elements] in Parrish et al. Reversal of this rejection of claim 20 is requested for this reason, and also for the reasons given above in connection with claim 16.

This is not found persuasive because as shown in the rejection of claim 20 above, because Parrish et al. shows at least DCM2 allocated in two out of three nodes of fig. 8, an access to DCM2 will be propagated to two out of three nodes, and two is less than all (three nodes) and more than one node.

On page 17 of the brief, applicant argues:

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"The Examiner suggest (Office Action dated march 28, 2003, page 14) that this limitation [less than all but more than one] is found in Parrish at Fig. 8B-8D, with "a local address of DCM2 allocated in two different nodes." It appears to the undersigned, however, that the addresses to which the Examiner refers (768K to 1280K in Fig. 8B, and 1024K to 1536K in Fig. 8D) cannot possibly represent global addresses. It appears to the undersigned that these are local addresses. As such, an overlap in the start and end points of each locally defined range would not mean anything about global addressing."

This is not found persuasive because applicant's arguments are completely unrelated to the claim language at issue. The claim language recites that "the propagating step comprises propagating ... [to] less than all and more than one". The fact that local addresses in two different nodes differ is unrelated to how the messages were propagated. As defined by Parrish et al., DCM2 relates to a memory area that is shared between two nodes (col. 1 lines 7-10, col. 5 lines 11-25, col. 14 lines 42-45). Accordingly, changes to the memory area represented by DCM2 are propagated to two nodes (col. 12 lines 10-35), Node A and Node C, which is less than the total number of nodes (three) in the system of fig. 8. Accordingly, the claim language is met by the reference.

On page 17-18 applicant then continues to argue about claim 20 by referring to Parrish et al.'s global memory partition and reserving a physical address. However, exactly as above, none of these arguments relate to the claim language at issue, which claims how the message propagation occurs. Additionally, DCM is defined by Parrish et al. as Distributed Common Memory, so applicant's arguments regarding Parrish et al.'s Global Memory and reserving systems are unrelated to the DCM cited against claim 20.

On pages 18-19 of the brief, applicant argues:

"The rejection of claim 25 should be reversed for the same reasons as given above in connection with claim 16. As discussed above with respect to claim 20, the office actions do not point out where in Parrish this limitation of claim 25 ("less than all and more than one") may be found, and the undersigned has been unable to find this limitation in Parrish.

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This is not found persuasive because as discussed above in connection with claim 25, not only does Parrish et al. indeed teach the language of the claim [further limitation of the propagating step] but as well applicant's arguments against Parrish et al. are unrelated to the specific claim language of claim 20.

On page 20 of the brief, applicant argues:

"The rejection of claim 27 should be reversed for the same reason as given above for claim 16, namely the "bus/message-passing-network" distinction. As discussed above with respect to claim 20, the office actions do not point out where in Parrish this limitation of claim 27 ("less than all and more than one") may be found, and the undersigned has been unable to find this limitation in Parrish."

This is not found persuasive because as detailed above, applicant's special secret unstated distinction between bus and message-passing-network can not be relied upon to differentiate the claim language from the reference. As detailed above in the claim construction section, applicant's specification and claims provide no guidance as to the meaning of "message-passing communications network" and therefore only the ordinary commonly accepted meaning can apply to this term in the claims. As that ordinary commonly accepted meaning does not exclude Parrish et al.'s INTERCONNECT BUS from that definition, Parrish et al.'s INTERCONNECT BUS is indeed a "message-passing communications network" to the extent necessary to read upon the claim language. Additionally, as pointed out above in the rejection of claim 20 and response to argument regarding claim 20, not only does Parrish et al. teach the claimed language of propagation, but applicant's arguments against the reference are unrelated to the text of the claim language.

On page 22 of the brief, applicant argues:

"The rejection of claim 29 should be reversed for the same reason as given above for claim 16, namely the "bus/message-passing-network" distinction. As discussed above with respect to claim

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20, it appears to the undersigned that the office actions do not point out where in Parrish this limitation of claim 29 ("less than all and more than one") may be found, and the undersigned has been unable to find this limitation in Parrish."

This is not found persuasive for the identical reasons as the response to claim 27 above, because this argument is identical to the argument regarding claim 27.

On page 23 of the brief, applicant argues:

"The rejection of claim 33 should be reversed for the same reason as given above for claim 16, namely the "bus/message-passing-network" distinction. But it should be noted that this claim differs from claim 16 in expressly reciting in three places the fact of the message-passing communications network being quite different from a common bus".

This is not found persuasive for the identical reasons given in the response to claim 27 above, because this argument is 50% identical to the argument regarding claim 27. The second half of applicant's argument, referring to the supposed "express reciting in three places the fact of the message-passing communications network being quite different from a common bus" is referring to the claim language construct of "not solely". As was detailed in the claim construction section, "not solely" means "not exclusively" and as detailed in the rejection of claim 33 because Parrish et al.'s INTERCONNECT BUS was defined by Parrish et al. to operate as both a common bus and a message-passing bus, it is not exclusively a common bus, i.e., not limited to functioning only as a common bus, and therefore is "not solely a common bus". Additionally, as detailed in the rejection of the claims above, Parrish et al.'s Interconnect bus reads upon both possible interpretations of applicant's claim language construct, the argued construct of further limiting the "message-passing communications network" and the literal claim language construct of the communications managers connected to two different buses.

On page 24 of the brief, applicant argues:

"The rejection of claim 34 should be reversed for the same reason as given above for claim 16,

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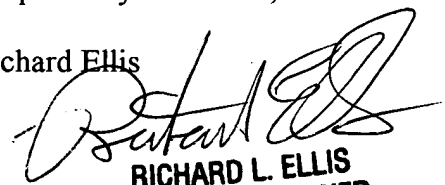
namely the "bus/message-passing-network" distinction. But it should also be noted that this claim differs from claim 16 in expressly reciting in three places the fact of the message-passing communications network being quite different from a common bus."

This is not found persuasive for the identical reasons as the response to claim 33 above, because this argument is identical to the argument regarding claim 33.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Richard Ellis




RICHARD L. ELLIS
PRIMARY EXAMINER

April 27, 2005

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